

Ultra puts Chip-rack to the test

"IF YOU don't put a lot of money up front in the connector industry, you shouldn't be in it." So says Ray Willis, the marketing director of Ultra Electronic Components in High Wycombe.

The major proportion of UECL's product range is connectors for PCB applications, but the company plans to increase its customer base by introducing new products and marketing strategies.

So when Mike Anstey and Dave Brown went knocking on Ultra's door with their innova-

Mary Fagan looks at Ultra's latest connector plans

nal connections, the DIL package is already unacceptable.

The most obvious alternative is the leadless chip carrier type of package. The use of all four sides of the package and the reduction in contact pitch mean that the size of the package is reduced and that a larger number of contact points can be accommodated.

connector companies, has a keen interest in the development of packaging techniques as they will affect all connector design.

As Ray Willis comments: "Technology changes will cause a reduction in the use of present design connectors. We must be in packaging if we are to maintain our growth for the future." Mike Anstey's ideas represent "an exciting new development," which Ultra hope will ensure that growth.

The basic concept involves constructing a carrier which has connecting pads on both upper and lower surfaces. This means that the number of available contacts per carrier is doubled, and that the chip carrier itself becomes a functional part of a three-dimensional interconnection system.

The semiconductor die can be connected to pads on the upper and lower surfaces and signals can enter on one surface of a carrier at a particular point and then emerge or continue from the other surface at another appropriate point.

The ability to re-route power or signal within a carrier structure 'modularises' the complexity of a printed circuit board as the re-routing now implemented by the PCB is effectively incorporated into the basic semiconductor package.

As a result, it becomes feasible to consider much simpler, standardised methods of interconnection than the customised board.

Anstey and Brown then developed the idea of mounting the chip carriers in a racking structure in order to enable cooling from both sides and to do away with the problems of



At the UECL factory in High Wycombe, Ray Willis and Mike Anstey examine a scaled-up model of the racking structure at one stage of its evaluation.

thermal mismatch which occur when trying to mount flat packs on to flat boards.

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the constant reprogramming needed with pick-and-place mechanisms. The reduced costs accruing from this ease of automation should enhance the acceptability of the system.

There are, of course, alternatives. Ultra Electronics is also looking at high-density connectors and press-fit packaging using multilayer boards. "It's a shared problem," Willis said. "Every connector manufac-

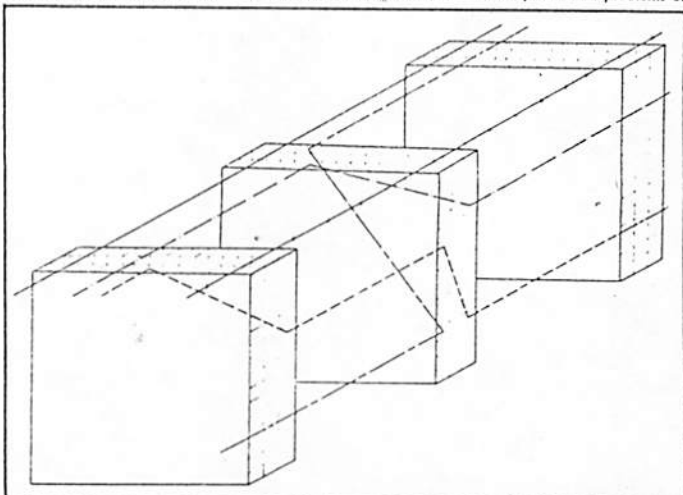
turer is investigating connectors for leadless chip carriers and have ideas on how to go about it. But this is a new approach, so why copy everyone else?"

For Mike Anstey and Dave Brown, who together form ICDC Ltd, the three years which they have devoted to developing the "Chiprack" scheme is just beginning to prove worthwhile.

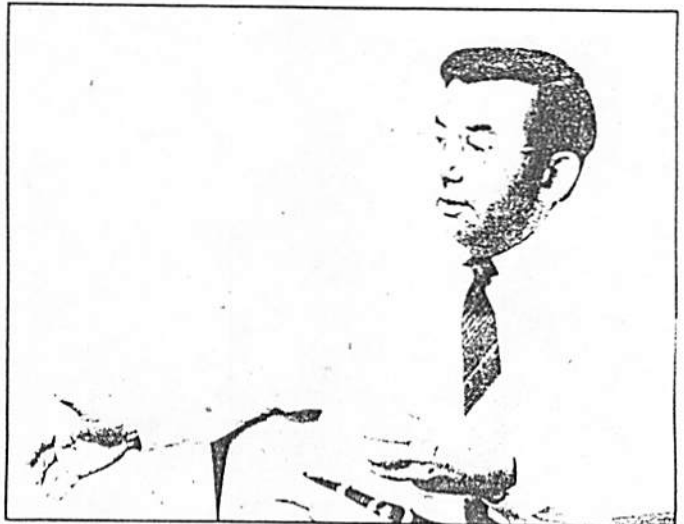
Chip carriers are currently interconnected in a similar manner to the DIL, via PCB. If greater complexity than that which is provided by a single PCB is required, then multilayer boards with vias running between the layers are used.

The problem here is that the costings of printed circuit boards increase dramatically when the 2-D interconnection of a single PCB is extended to three dimensions by the vertical interconnections between the layers of multilayer boards.

Ultra, like most other



A high degree of complexity is made possible in two ways: The double-sided carrier means that power and signal input on one side of the carrier can, to a certain extent, emerge in a different pattern at the other side. Special carriers containing crossover networks can be inserted into the rack to reroute power or signal at any point. However, for some applications, such as memory arrays, a through BUS structure without crossovers will be sufficient.



Ray Willis, marketing director of Dowty-UECL. The firm, he feels, has always been considered solid and respectable, but not given enough credit for its policy of innovation

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Packaging concept

a contract to evaluate "the market acceptance of chip racking as a packaging concept taken in relation to the cost of production."

The initial investigation is likely to take about 12 to 15 months and the company is willing to invest up to £250,000 in the project.

Ultra will also be talking to the major semiconductor houses to gauge their acceptance of the ideas and to enrol their help in the production of chips that are compatible with the system.

Their confidence in the successful outcome of the project seems well founded. One of the main advantages of the chip racking system is the complexity of interconnection which can be achieved.

Besides the limited scope for re-routing which will be available within individual chip packages, 'dummy chips', which function purely as cross-

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Entrepreneur, Mike Anstey of ICDC - happy to find a company so willing to listen to new ideas.

Software control

over networks, can be incorporated into the racking system.

By making use of these networks, either standard or customised depending on the application, any degree of complexity is possible. It could even be possible, in the future, to have the internal interconnections re-routed under software control.

The other important aspect is that chip racking lends itself ideally to automated manufacturing techniques. The actual racking structure and the physical form of the chip carriers remain constant.

This means that the assembly process, is the same, whatever the product, doing away with

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